IN THE CLAIMS:

Please amend the claims as follows:

1. (Cancelled)

2. (Currently amended) The semiconductor device of Claim [[1]] 6, wherein the dual use pads have a shape compatible with both assembly and connection with the probe, and the assembly pads have a shape compatible with only assembly.

3-4. (Cancelled)

5. (Currently amended) A semiconductor device having a plurality of pads above a main surface of a semiconductor substrate as terminals for external connection, wherein

the plurality of pads include dual use pads which are used in both a probing test and assembly, assembly pads which are not used in the probing test, and probing test pads which are not used in assembly,

the dual use pads and the probing test pads are provided in a first area above the main surface of the semiconductor substrate, an application of pressure by a probe during the probing test being permitted in the first area,

the assembly pads are provided in a second area above the main surface of the semiconductor substrate, the application of pressure by the probe during the probing test not being permitted in the second area,

~~The semiconductor device of Claim 4, wherein~~

the dual use pads have a shape compatible with both assembly and connection with the probe,

the assembly pads have a shape compatible with only assembly,

the probing test pads have a shape compatible with only connection with the probe, and

a measurement in a pad pitch direction of the shape compatible with only connection with the probe is smaller than a measurement in a pad pitch direction of the shape compatible with only assembly.

6. (Currently amended) A semiconductor device having a plurality of pads above a main surface of a semiconductor substrate as terminals for external connection, wherein

the plurality of pads include dual use pads which are used in both a probing test and assembly, assembly pads which are not used in the probing test, and probing test pads which are not used in assembly,

the dual use pads and the probing test pads are provided in a first area above the main surface of the semiconductor substrate, an application of pressure by a probe during the probing test being permitted in the first area,

the assembly pads are provided in a second area above the main surface of the semiconductor substrate, the application of pressure by the probe during the probing test not being permitted in the second area, and

~~The semiconductor device of Claim 3, wherein~~ the first area corresponds to the area above the peripheral region of the main surface of the semiconductor substrate, and the dual use pads and the probing test pads are arranged alternately and along the periphery of the main surface of the semiconductor substrate.

7-13. (Cancelled)